WHAT IS CLAIMED IS:

1. A sigma-delta modulator, comprising:

a discrete time circuit operable to:

receive a digital feedback signal and an input signal, the input signal comprising information and one or more analog input currents;

convert the digital feedback signal into an analog feedback signal during a first discrete time; and

sum the analog feedback signal and the one or more analog input currents during a second discrete time to yield one or more summed signals;

a continuous time circuit comprising a plurality of passive elements, the continuous time circuit coupled to the discrete time circuit and operable to filter the one or more summed signals using a first-order filter and a second-order filter in order to generate one or more filtered signals, the first-order filter comprising one or more first passive elements of the plurality of passive elements, the second-order filter comprising one or more second passive elements of the plurality of passive elements; and

a quantizer coupled to the continuous time circuit and operable to generate the digital signal using the one or more filtered signals, the digital signal comprising the information.

2. The sigma delta modulator of Claim 1, further comprising a transconductance circuit operable to:

receive the input signal comprising the information, the input signal having one or more analog input voltages; and

convert the one or more analog input voltages into one or more analog input currents.

3. The sigma-delta modulator of Claim 1, wherein the discrete time circuit is further operable to convert the digital feedback signal into an analog feedback signal using a reference voltage, the reference voltage supplied by a reference capacitor, the reference capacitor charged to the reference voltage during the first discrete time.

4. The sigma-delta modulator of Claim 1, wherein:

the one or more first passive elements associated with the first order filter comprises a first capacitor; and

the one or more second passive elements associated with the second order filter comprises a second capacitor and a resistor.

5. The sigma-delta modulator of Claim 1, wherein:

the discrete time circuit comprises a reference capacitor, the reference capacitor associated with a reference capacitance;

the one or more first passive elements associated with the first order filter comprises a first capacitor, the first capacitor associated with a first capacitance; and

the ratio between the first capacitance and the reference capacitance is substantially greater than one.

6. The sigma-delta modulator of Claim 1, wherein:

the one or more second passive elements associated with the second order filter comprises a second capacitor and a resistor, the second capacitor associated with a second capacitance, the resistor associated with a resistance; and

the second capacitance and the resistance selected according to a frequency response, the frequency response corresponding to a direct current frequency.

7. The sigma-delta modulator of Claim 1, wherein the quantizer comprises a comparator operable to generate the digital signal using the one or more filtered signals by:

amplifying the one or more filtered signals; and

comparing the one or more filtered signals to each other to quantize an error associated with the input signal and the digital signal.

8. The sigma-delta modulator of Claim 1, wherein the output of the quantizer is coupled to the discrete time circuit in order to form a passive feedback loop, the passive feedback loop operable to convert the digital signal into an analog feedback signal.

9. A method for converting an input signal into a digital signal, comprising:

receiving a digital feedback signal and an input signal at a discrete time circuit, the input signal comprising information and one or more analog input currents;

converting the digital feedback signal into an analog feedback signal during a first discrete time;

summing the analog feedback signal and the one or more analog input currents during a second discrete time to yield one or more summed signals;

filtering the one or more summed signals at a continuous time circuit in order to generate one or more filtered signals, the continuous time circuit comprising a first-order filter and a second-order filter, the first-order filter comprising one or more first passive elements of the plurality of passive elements, the second-order filter comprising one or more second passive elements of the plurality of passive elements; and

generating the digital signal using the one or more filtered signals, the digital signal comprising the information.

10. The method of Claim 9, further comprising:

receiving at a transconductance circuit the input signal comprising the information, the input signal having one or more analog input voltages; and

converting the one or more analog input voltages into the one or more analog input currents.

11. The method of Claim 9, wherein converting the digital feedback signal into an analog feedback signal during the first discrete time further comprises using a reference voltage, the reference voltage supplied by a reference capacitor, the reference capacitor charged to the reference voltage during the first discrete time.

12. The method of Claim 9, wherein:

the one or more first passive elements associated with the first order filter comprises a first capacitor; and

the one or more second passive elements associated with the second order filter comprises a second capacitor and a resistor.

13. The method of Claim 9, wherein:

the discrete time circuit comprises a reference capacitor;

the one or more first passive elements associated with the first order filter comprises a first capacitor; and

the ratio between the first capacitor and the reference capacitor is substantially greater than one.

14. The method of Claim 9, wherein:

the one or more second passive elements associated with the second order filter comprises a second capacitor and a resistor, the second capacitor associated with a second capacitance, the resistor associated with a resistance; and

the second capacitance and the resistance selected according to a frequency response, the frequency response corresponding to a direct current frequency.

15. The method of Claim 9, wherein generating the digital signal using the one or more filtered signals further comprises:

amplifying the one or more filtered signals; and

comparing at a comparator the one or more filtered signals to each other to quantize an error associated with the input signal and the digital signal.

16. The method of Claim 9, wherein the output of the quantizer is coupled to the discrete time circuit in order to form a passive feedback loop, the passive feedback loop operable to convert the digital signal into an analog feedback signal.

17. A sigma-delta modulator, comprising:

means for receiving a digital feedback signal and an input signal at a discrete time circuit, the input signal comprising information and one or more analog input currents;

means for converting the digital feedback signal into an analog feedback signal during a first discrete time;

means for summing the analog feedback signal and the one or more analog input currents during a second discrete time to yield one or more summed signals;

means for filtering the one or more summed signals at a continuous time circuit in order to generate one or more filtered signals, the continuous time circuit comprising a first-order filter and a second-order filter, the first-order filter comprising one or more first passive elements of the plurality of passive elements, the second-order filter comprising one or more second passive elements of the plurality of passive elements; and

means for generating the digital signal using the one or more filtered signals, the digital signal comprising the information.

18. A sigma-delta modulator, comprising:

a discrete time circuit operable to:

receive a digital feedback signal and an input signal, the input signal comprising information and one or more analog input currents;

convert the digital feedback signal into an analog feedback signal during a first discrete time using a reference voltage, the reference voltage supplied by a reference capacitor, the reference capacitor charged to the reference voltage during the first discrete time; and

sum the analog feedback signal and the one or more analog input currents during a second discrete time to yield one or more summed signals, the discrete time circuit further comprising a reference capacitor, the reference capacitor associated with a reference capacitance;

a continuous time circuit comprising a plurality of passive elements, the continuous time circuit coupled to the discrete time circuit and operable to filter the one or more summed signals using a first-order filter and a second-order filter in order to generate one or more filtered signals, the first-order filter comprising one or more first passive elements of the plurality of passive elements, the second-order filter comprising one or more second passive elements of the plurality of passive elements, the one or more first passive elements associated with the first order filter comprising a first capacitor, the one or more second passive elements associated with the second order filter comprising a second capacitor and a resistor, the ratio between the first capacitance and the reference capacitance is substantially greater than one;

a quantizer coupled to the continuous time circuit and operable to generate the digital signal using the one or more filtered signals, the digital signal comprising the information; and

a transconductance circuit operable to:

receive the input signal comprising the information, the input signal having one or more analog input voltages; and

convert the one or more analog input voltages into one or more analog input currents.

19. The sigma-delta modulator of Claim 18, wherein:

the one or more second passive elements associated with the second order filter comprises a second capacitor and a resistor, the second capacitor associated with a second capacitance, the resistor associated with a resistance; and

the second capacitance and the resistance selected according to a frequency response, the frequency response corresponding to a direct current frequency.

20. The sigma-delta modulator of Claim 18, wherein the quantizer comprises a comparator operable to generate the digital signal using the one or more filtered signals by:

amplifying the one or more filtered signals; and

comparing the one or more filtered signals to each other to quantize an error associated with the input signal and the digital signal, wherein the output of the comparator is coupled to the discrete time circuit in order to form a passive feedback loop, the passive feedback loop operable to convert the digital signal into an analog feedback signal.